Amendments to the Claims:

Please amend the claims as shown in the Listing of Claims below. This Listing of Claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-6. (Canceled)

7. (Previously Presented) An electronic device having a main processing unit and a plurality of sub-processing units, wherein each of the main processing unit and the plurality of sub-processing units includes a first bus-connecting unit for connecting a bus for data input, a second bus-connecting unit for connecting a bus for data output, and means for processing a process request packet directed to itself, and for bypassing a process request packet, directed to the other one and input from the first bus-connecting unit, to the second bus-connecting, and wherein the main processing unit further includes a signal terminal for sending test signals to each of the plurality of sub-processing units, the signal terminal being directly connected to each of the plurality of the sub-processing units, and wherein upon receiving the test signal, each of the plurality of sub-processing units outputs an interrupt packet via the second bus-connecting unit, and wherein a data bus in a loop is formed that connects the main processing unit and the sub-processing units, said electronic device comprising:

determining means for outputting, to the second bus-connecting unit in the main processing unit, a command packet bypassed by all of the plurality of sub-processing units, and returned to the first bus-connecting unit of the main processing unit, to determine whether an error exists on the data bus in the loop, and

identifying means for, in a case where an error exists, sending the test signal to each of the sub-processing units via the signal terminal of the main processing unit,

wherein the identifying means determines whether the interrupt packet for the test signal has been received in order to identify a location of said error.

8. (Previously Presented) An electronic device according to Claim 7, wherein, in a case where the error is determined by said determining means, said identifying means performs the

processes of sending the test signal and determining the reception of the interrupt packet from the sub-processing units in order, beginning from the sub-processing unit arranged in a downstream in the loop connection, and, thereby, identifies the error location.

9. (Previously Presented) An electronic device having a main processing unit and a plurality of sub-processing units, wherein each of the main processing unit and the plurality of sub-processing units includes a first bus-connecting unit for connecting a bus for data input, a second bus-connecting unit for connecting a bus for data output, and means for processing a process request packet, directed to itself and input from the first bus-connecting unit, in accordance with the request, and for bypassing a process request packet, directed to the other one and input from the first bus-connecting unit, to the second bus-connecting unit, and wherein the main processing unit further includes a signal terminal for test signals to be received from each of the plurality of sub-processing units, the signal terminal being directly connected to each of the plurality of the sub-connecting units, and wherein each of the plurality of sub-processing units further includes a test signal output unit for outputting a test signal to the main processing unit when an interrupt packet for test has been received via the first bus-connecting unit, and wherein a data bus in a loop is formed upon the mutual connection to each of the main processing unit and the plurality of sub-processing units via the each first bus-connecting unit and the each second bus-connecting unit, said electronic device comprising:

determining means for outputting, to the second bus-connecting unit in the main processing unit, a command packet bypassed by all of the plurality of sub-processing units, determining whether the command packet has been received from the first bus-connecting unit of the main processing unit, and for determining whether an error exists on the data bus in the loop, and

identifying means for, in a case where the error is determined by said determining means, sending the interrupt packet for the test signal to the second bus-connecting unit of the main processing unit, determining whether the interrupt packet has been received, and identifying a location of the error.

10. (Previously Presented) An electronic device according to Claim 9, wherein, in a case where the error is determined by said determining means, said identifying means performs the

processes of sending the interrupt packet and determining the reception of the interrupt packet to the sub-processing units in order from the sub-processing unit arranged in a downstream in the loop connection, and, thereby, identifies the error location.

11. (Previously Presented) A method for diagnosing an error in an electronic device having a main processing unit and a plurality of sub-processing units, wherein each of the main processing unit and the plurality of sub-processing units includes a first bus-connecting unit for connecting a bus for data input, a second bus-connecting unit for connecting a bus for data output, and means for processing a process request packet, directed to itself and input from the first bus-connecting unit, in accordance with the request, and for bypassing a process request packet, directed to the other one and input from the first bus-connecting unit, to the second bus-connecting unit, and wherein the main processing unit further includes a signal terminal for test signals to be sent to each of the plurality of sub-processing units, the signal terminal being directly connected to each of the plurality of the sub-connecting units, and wherein each of the plurality of sub-processing units further includes an input unit for inputting the test signal and an output unit for outputting an interrupt packet for test via the second bus-connecting unit when the test signal has been received, and wherein a data bus in a loop is formed upon the mutual connection to each of the main processing unit an the plurality of sub-processing units via the each first bus-connecting unit and the each second bus-connecting unit, said method comprising the steps of:

outputting, to the second bus-connecting unit in the main processing unit, a command packet bypassed by all of the plurality of sub-processing units, determining whether the command packet has been received or not from the first bus-connecting unit of the main processing unit, and for determining whether an error exists or not on the data bus in the loop, and

sending, in a case where the error is determined by said determining means, the test signal to each of the sub-processing units via the signal terminal of the main processing unit, determining whether the interrupt packet for the test signal has been received or not, and identifying a location of the error.

12. (Previously Presented) A method according to Claim 11, wherein, in a case where the

error is determined in said determining step, said identifying step performs the processes of sending the test signal and determining the reception of the interrupt packet to the sub-processing units in order from the sub-processing unit arranged in a downstream in the loop connection, and, thereby, identifies the error location.

13. (Previously Presented) A method for diagnosing an error in an electronic device having a main processing unit and a plurality of sub-processing units, wherein each of the main processing unit and the plurality of sub-processing units includes a first bus-connecting unit for connecting a bus for data input, a second bus-connecting unit for connecting a bus for data output, and means for processing a process request packet, directed to itself and input from the first bus-connecting unit, in accordance with the request, and for bypassing a process request packet, directed to the other one and input from the first bus-connecting unit, to the second bus-connecting unit, and wherein the main processing unit further includes a signal terminal for test signals to be received from each of the plurality of sub-processing units, the signal terminal being directly connected to each of the plurality of the sub-connecting units, and wherein each of the plurality of sub-processing units further includes a test signal output unit for outputting a test signal to the main processing unit when an interrupt packet for test has been received via the first bus-connecting unit, and wherein a data bus in a loop is formed upon the mutual connection to each of the main processing unit an the plurality of sub-processing units via the each first bus-connecting unit and the each second bus-connecting unit, said method comprising the steps of:

outputting, to the second bus-connecting unit in the main processing unit, a command packet bypassed by all of the plurality of sub-processing units, determining whether the command packet has been received or not from the first bus-connecting unit of the main processing unit, and for determining whether an error exists or not on the data bus in the loop, and

sending, in a case where the error is determined by said determining means, the interrupt packet for the test signal to the second bus-connecting unit of the main processing unit, determining whether the interrupt packet has been received or not, and identifying a location of the error.

14. (Previously Presented) A method according to Claim 13, wherein, in a case where the

error is determined in said determining step, said identifying step performs the processes of sending the interrupt packet and determining the reception of the interrupt packet from the sub-processing units in order from the sub-processing unit arranged in a downstream in the loop connection, and, thereby, identifies the error location.

15. (Canceled)

16. (Canceled)

17. (Previously Presented) A method for determining the location of an error within an electronic device having a main processing and first and second sub-processing units, wherein the main processing unit and first sub-processing unit are coupled by a first data bus, and wherein the first and second sub-processing units are coupled by a second data bus, and the second and main sub-processing units are coupled by a third data bus, the method comprising:

generating a data packet from the main processing unit via the first, second and third data buses back to the main processing unit;

determining that an error exists if the data packet is not returned to the main processing unit within a predetermined time;

in the case that said error exists, generating a test signal via direct connections from the main processing unit to each of the first and second sub-processing units; and

transmitting a test packet from each of said sub-processing units via the second and third data buses to the main processing unit in order to determine the location of said error.